ABSTRACT

An elastic buffer structure and process to avoid overflow or underflow in serial protocol communications using spread spectrum transmit and receive clocks or other separate transmit and receive clocks which may be running at different frequencies. Overflow and underflow are averted by storing received data in a FIFO at different addresses using a receive address pointer incremented at a receive clock rate. Other circuitry senses which addresses have nonessential primitives or nonessential data that can be deleted. Data is transmitted out of the FIFO at a transmit clock rate using a transmit address pointer incremented at the transmit clock rate. Control logic compares the transmit pointer to the receiver pointer, and when the distance between the pointers becomes too large or two small, inserts additional nonessential primitives or nonessential data or deletes nonessential primitives or nonessential data so as to maintain the distance between the pointers at a constant, selected value.